Amendments to the Claims:

This listing of claims will replace all prior versions and listings of claims in the application:

Listing of Claims:

Claim 1 (withdrawn): A process of designing an integrated circuit comprising:

determining a specification for the integrated circuit;

mapping functions to the specification, the functions being comprised of groups; and

determining the placement of the functions in a layout.

Claim 2 (withdrawn): The process of designing an integrated circuit of claim 1 wherein the functions are of a plurality of predefined sizes and shapes.

Claim 3 (withdrawn): The process of designing an integrated circuit of claim 2 wherein the groups are of a plurality of predefined sizes and shapes.

Claim 4 (withdrawn): The process of designing an integrated circuit of claim 3 wherein the groups have predefined interconnection points.

Claim 5 (withdrawn): The process of designing an integrated circuit of claim 4 wherein the groups each provide one of a plurality of logic functions.

Claim 6 (withdrawn): The process of designing an integrated circuit of claim 5 wherein multiple groups, each of a different size and shape, provide the same logic function.

Claim 7 (withdrawn): The process of designing an integrated circuit of claim 6 further comprising mapping groups to the specification and determining placement of the groups in the layout.

Claim 8 (withdrawn): The process of designing an integrated circuit of claim 7 wherein the groups define a physical representation of a logic circuit.

Claim 9 (withdrawn): The process of designing an integrated circuit of claim 8 wherein the groups are defined by GDSIII files.

Claim 10 (withdrawn): The process of designing an integrated circuit of claim 9 wherein the groups are comprised of on the order of 1000 gates.

Claims 11-26 (canceled)

Claim 27 (withdrawn): A process of designing an electronic logic system, the process comprising:

mapping groups to a functional description, the groups being comprised of up to 5000 gates, the groups being partitioned into data path groups, control groups, memory groups, I/O groups, and analog groups;

testing functional models of the mapped groups to verify the functional correctness of the mapping of groups to the functional description;

performing timing, area, and power estimation using detailed physical models of the mapped groups; and

importing implementation files into the design.

Claim 28 (withdrawn): The process of designing an electronic logic system of claim 27 wherein the groups are predefined in terms of behavior, timing, power, and physical layout.

Claim 29 (withdrawn): The process of designing an electronic logic system of claim 28 wherein different sets of groups implement different functions.

Claim 30 (withdrawn): The process of designing an electronic logic system of claim 29 wherein groups within a set of groups implementing a function implement different behavior.

Claim 31 (withdrawn): The process of designing an electronic logic system of claim 29 wherein groups within a set of groups implementing a function have different physical layouts.

Claim 32 (withdrawn): The process of designing an electronic logic system of claim 29 wherein groups within a set of groups implementing a function have different power usage.

Claim 33 (new): A method of designing an integrated circuit comprising:

creating a netlist design for each of a set of sub-circuits, each sub-circuit performing an electronic operation and having at least 300 gates;

creating a physical layout for each such sub-circuit which layout includes information defining the physical position of all components of the sub-circuit, and locations on each such sub-circuit for interconnecting such sub-circuit to at least one other circuit;

defining desired electrical interconnections among all of the components of the sub-circuit, the electrical connections being defined on fewer than all layers available for the provision of interconnections in an integrated circuit to be designed later;

defining interconnection information for providing electrical connections as needed among such components;

optimizing the design and layout for each such sub-circuit to obtain a desired level of operating speed for such sub-circuit independently of any use of such sub-circuit with any other sub-circuit;

storing such optimized design for later use in conjunction with other sub-circuits and other circuits;

creating a netlist design for the integrated circuit which includes at least two sub-circuits previously optimized and stored;

creating a physical layout for the integrated circuit by placing the at least two sub-circuits on a design in proximity to each other; which layout includes information defining the

physical position of the at least two sub-circuits and the locations on each such sub-circuit for interconnecting such sub-circuit to at least one other circuit; and

defining desired electrical interconnections among the sub-circuits, the electrical connections being defined entirely on layers other than the layers used for the desired electrical interconnections among the components of the sub-circuits.

Claim 34 (new): The method of claim 33 wherein in the step of defining desired electrical interconnections among all of the components of the sub-circuit, the electrical connections being defined on fewer than all layers available for the provision of interconnections in an integrated circuit to be designed later, at least one layer of the electrical interconnections does not include both power and clock signals.

Claim 35 (new): The method of claim 33 wherein the plurality of layers are each layers having electrically conductive material thereon, with vias between at least two adjoining layers.

Claim 36 (new): The method of claim 33 wherein each sub-circuit has a predefined size and shape.

Claim 37 (new): The method of claim 33 wherein each sub-circuits has predefined interconnection locations for connecting that sub-circuit to at least one other sub-circuit.

Claim 38 (new): The method of claim 37 wherein each sub-circuit provides one of a plurality of logic functions.

Claim 39 (new): The method of claim 38 wherein at least two sub-circuits having different size and shape provide the same logic function.

Claim 40 (new): The method of claim 33 wherein each sub-circuit comprises a physical representation of a logic circuit.

Claim 41 (new): The method of claim 40 wherein each sub-circuit is defined by at least one GDSIII file.

Claim 42 (new): The method of claim 33 wherein each sub-circuit comprises on the order of 1000 gates.

Claim 43 (new): The method of claim 33 wherein no layer in the layers available for the provision of interconnections in an integrated circuit to be designed later includes both electrical connections for interconnecting components of the sub-circuit and electrical connections for connecting one sub-circuit to another.

Claim 44 (new): An integrated circuit comprising a plurality of circuit sub-circuits, the circuit sub-circuits containing on an order of magnitude of 1000 gates, the circuit sub-circuits having predefined connection points, each sub-circuit having interconnections within that sub-circuit on a plurality of layers of the integrated circuit, the plurality of layers being less than all of the layers, and wherein connections between the circuit sub-circuits are provided on a layer of the integrated circuit not used for the interconnections within a sub-circuit.

Claim 45 (new): The integrated circuit of claim 44 wherein the plurality of circuit sub-circuits include electrical connections within them solely on a first plurality of electrically conductive layers, and wherein clock and power signals are provided on electrically conductive layers other than the first plurality of electrically conductive layers.

Claim 46 (new): The integrated circuit of claim 44 wherein the clock and power signals are on the same layer.

Claim 47 (new): The integrated circuit of claim 45 wherein global routing signals among the plurality of sub-circuits are transferred among the sub-circuits on at least one electrically conductive layer other than the first plurality of electrically conductive layers and other than the layer used for the clock and power signals.

Claim 48 (new): An integrated circuit comprising:

a plurality of circuit sub-circuits each on the order of 1000 gates, the circuit sub-circuits having predefined connection points;

at least some of the circuit sub-circuits being amalgamated into sets of sub-circuits;

at least one trailer attached to a sub-circuit to provide physical translation of interface signals associated with the predefined connection points

Claim 49 (new): The integrated circuit of claim 48 wherein the trailer further provides buffering of the interface signals associated with the predefined connection points.

Claim 50 (new): The integrated circuit of claim 49 wherein the trailer further provides staging of the interface signals associated with the predefined connections points.

Claim 51 (new): The integrated circuit of claim 48 wherein the integrated circuit comprises a plurality of metal layers, with the plurality of circuit sub-circuits on a first plurality of metal layers and clock and power signals on metal layers other than the first plurality of metal layers.

Claim 52 (new): The integrated circuit of claim 51 wherein the clock and power signals are provided on the same metal layer.

Claim 53 (new): The integrated circuit of claim 52 wherein global routing signals are provided on a metal layer other than the first plurality of metal layers and other than the metal layer of the clock and power signals.

Claim 54 (new): The integrated circuit of claim 53 wherein the global routing signals are provided on a plurality of metal layers.

Claim 55 (new): The integrated circuit of claim 48 wherein the sub-circuits comprise data path sub-circuits and memory sub-circuits.

Claim 56 (new): The integrated circuit of claim 55 wherein the sub-circuits further comprise control sub-circuits.

Claim 57 (new): The integrated circuit of claim 55 wherein the sub-circuits further comprise input/output sub-circuits.

Claim 58 (new): The integrated circuit of claim 55 wherein the sub-circuits further comprise analog sub-circuits.

Claim 59 (new): A process for designing an electronic logic system to be implemented as an integrated circuit, the process comprising:

mapping sub-circuits to a functional description, each sub-circuit comprising fewer than 5000 gates, the sub-circuits being partitioned into data path sub-circuits, control sub-circuits, memory sub-circuits, I/O sub-circuits, and analog sub-circuits;

testing functional models of the mapped sub-circuits to verify the functional correctness of the mapping of sub-circuits to the functional description;

performing timing, area, and power estimation using physical models of the mapped sub-circuits; and

importing implementation files into the design; and

laying out the design in a manner which places all interconnections within a sub-circuit on fewer than all of the layers of the integrated circuit.

Claim 60 (new): The process of designing an electronic logic system of claim 59 wherein the sub-circuits are predefined in terms of all of functionality, timing, power, and physical layout.

Claim 61 (new): The process of designing an electronic logic system of claim 60 wherein different sub-circuits implement different functions.

Claim 62 (new): The process of designing an electronic logic system of claim 60 wherein sub-circuits within a set of sub-circuits implementing a function implement different behavior.

Claim 63 (new): The process of designing an electronic logic system of claim 60 wherein sub-circuits within a set of sub-circuits implementing a function have different physical layouts.

Claim 64 (new): The process of designing an electronic logic system of claim 63 wherein sub-circuits within a set of sub-circuits implementing a function have different power consumption.